

SoC MMU

FLASH and PSRAM in ESP32* chips are attached through MMU which allows mapping different parts of FLASH and/or PSRAM into fixed address ranges. It's not very well documented for the ESP32 and I can't find any documentation for ESP32S3, so here's the bits scraped from docs, IDF source code, Espressif QEMU models and good old poking into registers-checking the effect.

ESP32

ESP32S3

512 32-bit entries starting at DR_REG_MMU_TABLE (0x600C5000). They control mapping of the virtual address ranges 0x3c000000..0x3e000000 connected to a DRAM bus and 0x42000000..0x44000000 connected to an IRAM bus. Bit 15 of the entry chooses PSRAM (if set) or FLASH (if clear), bit 14 of the entry indicates invalid entry (if set), lower bits choose one 64KByte page mapped to both DRAM and IRAM range.

From:
<http://wiki.osll.ru/> - **Open Source & Linux Lab**

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<http://wiki.osll.ru/doku.php/etc:users:jcmvbkbc:linux-xtensa:esp32s3:mmu>

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