Linux port for Xtensa

- Linux git tree: https://github.com/jcmvbkbc/linux-xtensa
- Build/test tools git tree: https://github.com/jcmvbkbc/xtensa-linux-test
- Toolchain build scripts/overlays git tree: https://github.com/jcmvbkbc/xtensa-toolchain-build
- Patch review check list
- Patch/pull request check list

TODO

- TIE coprocessors (23ae3f723c8996d47ef205e98cb7732bbde4775f)
- ptrace (support latest GDB) (617244763e19a4eebb4fabe41ba56eb1ccbdb049, 23ae3f723c8996d47ef205e98cb7732bbde4775f, ~~ff1b10f85a1176d1eb8df433434b717f6f0841d4~~ (already upstream), ~~a2b61af3328025d6069e8bf9ff36f5288e11dba9~~)
- ticket spinlocks
- dynamic ftrace
- kprobes
- fixes for debuggability (continuous stack trace over exceptions at least)

In Progress

- highmem on cores with aliasing cache
- support xtfpga audio hardware in ALSA
  - clock synthesizer
  - I2S interface
- deliver signals raised in double exceptions

Done

Highmem support

Done, in the -next

Limit PHY connected to OpenCores MAC to 10/100 MBits/s speeds

Done, in the mainline:

```
445a48c net: ethoc: don't advertise gigabit speed on attached PHY
a13aff0 net: ethoc: set up MII management bus clock
```

SMP support

Done, in the mainline:

```
99d5040 xtensa: keep a3 and excsave1 on entry to exception handlers
5515daa xtensa: fix arch spinlock function names
6235153 xtensa: update clockevent setup for SMP
cbd1de2 xtensa: move built-in PIC to drivers/irqchip
26a8e96 xtensa: add MX irqchip
f615136 xtensa: add SMP support
49b424f xtensa: implement CPU hotplug
```

Clean up and fix ISS networking

Done, in the mainline:

```
3f3cd60b xtensa: ISS: clean up iss-network driver
8c8ad85 xtensa: ISS: fix command line parameter name
358b181 xtensa: ISS: init network interface name before the probe
8991fd8 xtensa: ISS: drop IP setup, clean up MAC setup
f6ac5a1 xtensa: ISS: enable iss_net_set_mac
35e14b4 xtensa: ISS: always use fixed tuntap config
a6e16b9 xtensa: ISS: clean up diagnostic, increase verbosity
```

oprofile

~~8c502ca703956e56bf191774e4169752f0f71c8e, 7dd1d39e70769f2dd7a6a508d58b187ed8d1cb95~~

Done, in the mainline:

```
e6ffe17 xtensa: add support for oprofile
74f5bf0 xtensa: fix oprofile building as module
```

simdisk

~~1a955825662fa378d447b91485d9fe2438124b0a, 8bcbc3adb5c5bfdbd96078c1e68916be859c832d~~

Done, in the mainline:

```
b6c7e87 xtensa: ISS: add host file-based simulated disk
```

Medium level interrupts in less hacky way

~~489fb47c75772e3a41ef3e988eb0c0e512592085~~

Done, in the mainline:

```
2d1c645 xtensa: dispatch medium-priority interrupts
895666a xtensa: disable IRQs while IRQ handler is running
```

Interrupt management

Done, in the mainline:

```
2206d5d xtensa: add IRQ domains support
```

Cache aliasing aware mmap

Done, in the mainline:

```
de73b6b xtensa: avoid mmap cache aliasing
```

Atomics (arch/xtensa/include/asm/atomic.h, bitops.h, spinlock.h) and check for S32C1I

Merged in the eb0a9bf31fdbcee9463c0f42fbf4a292ef149a7d, pick up from individual files.

Done, in the mainline:

```
2f6ea6a xtensa: display s32c1i feature flag in cpuinfo
733536b xtensa: save and restore scompare1 SR on kernel entry
c622b29 xtensa: initialize atomctl SR
28570e8 xtensa: add trap_set_handler function
0027312 xtensa: add s32c1i sanity check
219b1e4 xtensa: add s32c1i-based atomic ops implementations
e5a9f6a xtensa: add s32c1i-based bitops implementations
71872b5 xtensa: add s32c1i-based spinlock implementations
599bf77 xtensa: fix mb and wmb definitions
```

Generic kernel_thread & friends

Done, in the mainline:

```
3306a72 xtensa: switch to generic kernel_thread()
f0a1bf0 xtensa: switch to generic kernel_execve()
dc241f2 xtensa: switch to generic sys_execve()
```

Support for Tensilica FPGA boards (xtfpga)

- [+] serial

- [+] ethernet
- [+] FLASH
- [-] audio

In the mainline:

```
0d456ba xtensa: add support for the XTFPGA boards
5584b4d xtensa: add XTFPGA DTS
```

Device trees support

Done, in the mainline:

```
da844a8 xtensa: add device trees support
```

MMU v3

Done, in the mainline:

```
e85e335 xtensa: add MMU v3 support
93e294a xtensa: document MMUv3 setup sequence
```

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