Cycle-accurate pipeline

5-stage pipeline:

- I instruction memory read;
- R instruction decode, register access;
- E ALU operation, effective address generation;
  - this stage may be delayed if it accesses a register affected by an earlier load instruction that has not yet reached M stage;
- M memory access;
- W register write back;

DSYNC < ESYNC < RSYNC < ISYNC

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http://wiki.osll.ru/ - **Open Source & Linux Lab**

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http://wiki.osll.ru/doku.php/etc:users:jcmvbkbc:qemu-target-xtensa:pipeline?rev=1312759658

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